



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

SEMESTER – I

S. No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D57102	CMOS Digital IC Design	PC	3	0	0	3
2.	21D06102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	3
3.	21D68101a 21D68101b 21D57104b	Program Elective – 1 Communication Buses and Interfaces Data Acquisition System Design FPGA Architectures and Applications	PE	3	0	0	3
4.	21D68102a 21D68102b 21D38201	Program Elective – 1 Low Power VLSI Design Nano-materials and Nanotechnology Network Security and Cryptography	PE	3	0	0	3
	21D57106	CMOS Digital IC Design Lab	PC	0	0	4	2
6.	21D06106	Microcontrollers and Programmable Digital Signal Processors Lab	PC	0	0	4	2
7.	21DRM101	Research Methodology and IPR	MC	2	0	0	2
8.	21DAC101a 21DAC101b 21DAC101c	Audit Course – I English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	AC	2	0	0	0
Total							18



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

SEMESTER – II

S.No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D57101	CMOS Analog IC Design	PC	3	0	0	3
2.	21D06201	Embedded System Design	PC	3	0	0	3
3.	21D68201a 21D68201b 21D68201c	Program Elective – III Pattern Recognition and Machine Learning Programming Languages for Embedded Software RF IC Design	PE	3	0	0	3
4.	21D06203a 21D68202a 21D57202	Program Elective – IV SoC Architecture System Design with Embedded Linux Physical Design Automation	PE	3	0	0	3
5.	21D57105	CMOS Analog IC Design Lab	PC	0	0	4	2
6.	21D06205	Embedded System Design Lab	PC	0	0	4	2
7.	21D06207	Technical seminar	PR	0	0	4	2
8.	21DAC201a 21DAC201b 21DAC201c	Audit Course – II Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	AC	2	0	0	0
Total							18



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

SEMSTER - III

S.No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D06204b 21D57204c 21D57204b	Program Elective – V Adhoc and Wireless Sensor Networks VLSI Signal Processing IoT and its Application	PE	3	0	0	3
2.	21DOE301b 21DOE301c 21DOE301e	Open Elective Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3
3.	21D68301	Dissertation Phase – I	PR	0	0	20	10
4.	21D68302	Co-curricular Activities					2
Total							18

SEMESTER - IV

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D68401	Dissertation Phase – II	PR	0	0	32	16
Total							16



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN	L	T	P	C
21D57102		3	0	0	3
Semester		I			
Course Objectives:					
- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles. - The course also involves analysis of performance metrics. - To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits. - To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.					
Course Outcomes (CO): Student will be able to					
- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS, - Estimate Delay and Power of Adders circuits. - Classify different semiconductor memories. - Analyze, design and implement combinational and sequential MOS logic circuits. - Analyze complex engineering problems critically in the domain of digital IC design for conducting research. - Solve engineering problems for feasible and optimal solutions in the core area of digital ICs					
UNIT - I		Lecture Hrs:			
MOS Design Pseudo NMOS Logic:Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.					
UNIT - II		Lecture Hrs:			
Combinational MOS Logic Circuits:MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.					
UNIT - III		Lecture Hrs:			
Sequential MOS Logic Circuits:Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop					
UNIT - IV		Lecture Hrs:			
Dynamic Logic Circuits:Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.					
UNIT - V		Lecture Hrs:			
Semiconductor Memories:Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.					
Textbooks:					
- Neil Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2010 - Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011. - CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.					
Reference Books:					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|--|
| <ol style="list-style-type: none">1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 20112. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI. |
|--|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE	L	T	P	C
21D06102	DIGITAL SIGNAL PROCESSORS	3	0	0	3
Semester		I			
Course Objectives:					
- To learn about ARM Microcontroller architectural features - To understand the ARM ‘C’ Programming for various applications - To study the DSP processor fundamentals and its development tools					
Course Outcomes (CO): Student will be able to					
- Learn about ARM Microcontroller architectural features - Understand the ARM ‘C’ Programming for various applications - Study the DSP processor fundamentals and its development tools					
UNIT - I		Lecture Hrs:			
ARM Cortex-Mx Processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.					
UNIT - II		Lecture Hrs:			
Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.					
UNIT - III		Lecture Hrs:			
LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.					
UNIT - IV		Lecture Hrs:			
Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family					
UNIT - V		Lecture Hrs:			
VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.					
Textbooks:					
- Joseph Yiu, “The definitive guide to ARM Cortex-M3”, Elsevier, 2nd Edition - Venkatramani B. and Bhaskar M. “Digital Signal Processors: Architecture, Programming and Applications” , TMH, 2nd Edition.					
Reference Books:					
- Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication. - Steve furber, “ARM System-on-Chip Architecture”, Pearson Education - Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley - Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	COMMUNICATION BUSES AND INTERFACES	L	T	P	C
21D68101a		3	0	0	3
Semester		I			
Course Objectives:					
- To understand the concepts of different types of serial buses. - To learn about CAN, PCIe and USB architecture - To learn about data streaming using serial communication protocols					
Course Outcomes (CO): Student will be able to					
- Understand the concepts of different types of serial buses. - Learn about CAN, PCIe and USB architecture - Learn about data streaming using serial communication protocols					
UNIT - I		Lecture Hrs:			
Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C , SPI					
UNIT - II		Lecture Hrs:			
CAN ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.					
UNIT - III		Lecture Hrs:			
PCIe Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.					
UNIT - IV		Lecture Hrs:			
USB Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.					
UNIT - V		Lecture Hrs:			
Data streaming Serial Communication Protocol- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.					
Textbooks:					
- A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005. - Serial Port Complete-COM Ports, USB Virtual Com Ports and Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,					
Reference Books:					
- USB Complete – Jan Axelson, Penram Publications. - PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	DATA ACQUISITION SYSTEM DESIGN	L	T	P	C
21D68101b		3	0	0	3
	Semester	I			
Course Objectives:					
• To understand the different types of communication interface buses. • To familiarize different methods of ADC's and DAC's characteristics, specifications • To study the software tools to develop the code and implementation for data acquisition system					
Course Outcomes (CO): Student will be able to					
Students will be able to					
• Understand the different types of communication interface uses. • Familiarize different methods of ADC's and DAC's characteristics, specifications • Study the software tools to develop the code and implementation for data acquisition system					
UNIT - I		Lecture Hrs:			
Fundamentals of Data Acquisition Systems, Sensors and Transducers, Signal conditioning - Introduction, Types of signal conditioning, Classes of signal conditioning, DAQ Hardware, DAQ Software, Communications Cabling, Parameters of a DAQ System.					
UNIT - II		Lecture Hrs:			
Data acquisition system configuration, Computer plug in I/O, Distributed I/O, Stand-alone or distributed loggers/controllers- Introduction, Methods of operation, Stand-alone logger/controller hardware, firmware & software design, Communications hardware interface, Host software, Considerations, internal systems, USB overall structure, PCMCIA card					
UNIT - III		Lecture Hrs:			
Data Acquisition Systems: Hardware-Introduction, Plug-in DAQ Systems, Converters A/D, Converters D/A, Amplifier, Multiplexer/De-multiplexer, Power Management, Timing System, Filtering, Memory Board, Bus Interface.					
UNIT - IV		Lecture Hrs:			
Communication Bus-Bus and FireWire, Serial Communications, Wireless, Ethernet and Bluetooth, GSM for Data Acquisition System, PCI and PCI Express, Standard VME.					
UNIT - V		Lecture Hrs:			
Design of Data Acquisition System: Introduction to the Design, Functional Design of high-Speed Computers-Based DAS, Portable DAS, Design Guidelines for High-Performance Multichannel. Software for Data Acquisition Systems, Introduction to LabVIEW, Android for DAQ, Design of Firmware, Example of Implementation of a Software.					
Textbooks:					
1. Maurizio Di Paolo Emilio "Data acquisition systems-from fundamentals to applied design" springer, 2013. 2. John Park and Steve Mackay "Practical Data acquisition for instrumentation and control systems" Elsevier, 2003.					
Reference Books:					
1. Robert H King, "Introduction to Data Acquisition with LabVIEW", 2nd edition, 2012, McGraw					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	FPGA ARCHITECTURES AND APPLICATIONS	L	T	P	C
21D57104b		3	0	0	3
	Semester	I			
Course Objectives:					
• To acquire knowledge about various architectures and device technologies of PLD's. • To comprehend FPGA Architectures. • To analyze System level Design and their application for Combinational and Sequential Circuits. • To familiarize with Anti-Fuse Programmed FPGAs. • To apply knowledge of this subject for various design applications.					
Course Outcomes (CO): Student will be able to					
• Acquire knowledge about various architectures and device technologies of PLD's. • Comprehend FPGA Architectures. • Analyze System level Design and their application for Combinational and Sequential Circuits. • Familiarize with Anti-Fuse Programmed FPGAs. • Apply knowledge of this subject for various design applications.					
UNIT - I		Lecture Hrs:			
Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.					
UNIT - II	Field Programmable Gate Arrays	Lecture Hrs:			
Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.					
UNIT - III		Lecture Hrs:			
SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.					
UNIT - IV		Lecture Hrs:			
Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.					
UNIT - V		Lecture Hrs:			
Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture					
Textbooks:					
1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.					
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.					
Reference Books:					
1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.					
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.					
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.					
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	LOW POWER VLSI DESIGN	L	T	P	C
21D68102a		3	0	0	3
	Semester	I			
Course Objectives:					
- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect - To implement Low power design approaches for system level and circuit level measures. - To design low power adders, multipliers and memories for efficient design of systems.					
Course Outcomes (CO): Student will be able to					
- Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect - Implement Low power design approaches for system level and circuit level measures. - Design low power adders, multipliers and memories for efficient design of systems.					
UNIT - I		Lecture Hrs:			
Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.					
UNIT - II		Lecture Hrs:			
Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.					
UNIT - III		Lecture Hrs:			
Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder’s Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.					
UNIT - IV		Lecture Hrs:			
Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.					
UNIT - V		Lecture Hrs:			
Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.					
Textbooks:					
1.CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.					
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.					
Reference Books:					
1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.					
2.Low Power CMOS Design – AnanthaChandrasekaran, IEEE Press/Wiley International, 1998.					
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	NANOMATERIALS AND NANOTECHNOLOGY	L	T	P	C
21D68102b		3	0	0	3
Semester		I			
Course Objectives:					
- To understand the basic idea behind the design and fabrication of nano scale systems. - To understand and formulate new engineering solutions for current problems and technologies for future applications. - To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.					
Course Outcomes (CO): Student will be able to					
- Understand the basic science behind the design and fabrication of nano scale systems. - Understand and formulate new engineering solutions for current problems and competing technologies for future applications. - Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development. - Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.					
UNIT - I		Lecture Hrs:			
Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.					
UNIT - II		Lecture Hrs:			
Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials.Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.					
UNIT - III		Lecture Hrs:			
Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.					
UNIT - IV		Lecture Hrs:			
Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT's - Multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT's, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs.					
UNIT - V		Lecture Hrs:			
Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane based application, polymer based application.					
Textbooks:					
- Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2nd edition, John Wiley and Sons, 2009. - I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008. - B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGrawHill Education 2012.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

(Established by Govt. of A.P., ACT No.30 of 2008)

ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Reference Books:

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borivoje Nikolic, 2nd Edition, PHI.



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	NETWORK SECURITY AND CRYPTOGRAPHY	L	T	P	C
21D38201		3	0	0	3
Semester		I			
Course Objectives:					
- To identify and utilize different forms of cryptography techniques. - To incorporate authentication and security in the network applications. - To distinguish among different types of threats to the system and handle the same.					
Course Outcomes (CO):					
- Identify and utilize different forms of cryptography techniques. - Incorporate authentication and security in the network applications. - Distinguish among different types of threats to the system and handle the same.					
UNIT - I		Lecture Hrs:			
Security: Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.					
UNIT - II		Lecture Hrs:			
Number Theory: Introduction, Fermat’s and Euler’s Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.					
UNIT - III		Lecture Hrs:			
Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.					
UNIT - IV		Lecture Hrs:			
Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.					
UNIT - V		Lecture Hrs:			
Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.					
Textbooks:					
- William Stallings, “Cryptography and Network Security, Principles and Practices”, Pearson Education, 3rd Edition. - Charlie Kaufman, Radia Perlman and Mike Speciner, “Network Security, Private Communication in a Public World”, Prentice Hall, 2ND Edition.					
Reference Books:					
1. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, “Security Architecture, Design Deployment and Operations”, RSA Pres,					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|--|
| <ol style="list-style-type: none">2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, “Inside Network Perimeter Security”, Pearson Education, 2 ndEdition3. Richard Bejtlich, “The Practice of Network Security Monitoring: Understanding Incident Detection and Response”, William Pollock Publisher, 2013. |
|--|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN LAB	L	T	P	C
21D57106		0	0	4	2
Semester		I			
Course Objectives:					
- To explain the VLSI Design Methodologies using any VLSI design tool. - To grasp the significance of various design logic Circuits in full-custom IC Design. - To explain the Physical Verification in Layout Extraction. - To fully appreciate the design and analyze of CMOS Digital Circuits. - To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.					
Course Outcomes (CO):					
- Explain the VLSI Design Methodologies using any VLSI design tool. - Grasp the significance of various design logic Circuits in full-custom IC Design. - Explain the Physical Verification in Layout Extraction. - Fully appreciate the design and analyze of CMOS Digital Circuits.					
Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.					
List of Experiments:					
The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology.					
1. Inverter Characteristics.					
2. NAND and NOR Gate					
3. XOR and XNOR Gate					
4. 2:1 Multiplexer					
5. Full Adder					
6. RS-Latch					
7. Clock Divider					
8. JK-Flip Flop					
9. Synchronous Counter					
10. Asynchronous Counter					
11.Static RAM Cell					
12. Dynamic Logic Circuits					
13. Linear Feedback Shift Register					
Lab Requirements:					
Software:					
Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software					
Hardware:					
Personal Computer with necessary peripherals, configuration and operating System.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB	L	T	P	C
21D06106		0	0	4	2
Semester		I			
Course Objectives:					
• To write the ARM ‘C’ programming for applications • To understand the interfacing of various modules with ARM 7/ ARM Cortex-M3 • To develop assembly and C Programming for DSP processors					
Course Outcomes (CO):					
• Install, configure and utilize tool sets for developing applications based on ARM processor core. • Design and develop the ARM7 based embedded systems for various applications. • Develop application programs on ARM and DSP development boards both in assembly and C. • Design and Implement the digital filters on DSP6713 processor. • Analyze the hardware and software interaction and integration.					
List of Experiments:					
Part A) Experiments to be carried out on Cortex-Mx development boards and using GNU tool-chain					
1. Blink an LED with software delay, delay generated using the SysTick timer.					
2. System clock real time alteration using the PLL modules.					
3. Control intensity of an LED using PWM implemented in software and hardware.					
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.					
5. UART Echo Test.					
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.					
7. Temperature indication on an RGB LED.					
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.					
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.					
10. System reset using watchdog timer in case something goes wrong.					
11. Sample sound using a microphone and display sound levels on LEDs.					
Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)					
12. To develop an assembly code and C code to compute Euclidian distance between any two points					
13. To develop assembly code and study the impact of parallel, serial and mixed execution					
14. To develop assembly and C code for implementation of convolution operation					
15. To design and implement filters in C to enhance the features of given input sequence/signal					
Software Requirements:					
Keil for ARM, Code Composer Studio					
Hardware Requirements:					
ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	RESEARCH METHODOLOGY AND IPR	L	T	P	C
21DRM101		2	0	0	2
Semester		I			
Course Objectives:					
- Identify an appropriate research problem in their interesting domain. - Understand ethical issues understand the Preparation of a research project thesis report. - Understand the Preparation of a research project thesis report - Understand the law of patent and copyrights. - Understand the Adequate knowledge on IPR					
Course Outcomes (CO): Student will be able to					
- Analyze research related information - Follow research ethics - Understand that today’s world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity. - Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular. - Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.					
UNIT - I		Lecture Hrs:			
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations					
UNIT - II		Lecture Hrs:			
Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.					
UNIT - III		Lecture Hrs:			
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.					
UNIT - IV		Lecture Hrs:			
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.					
UNIT - V					
New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.					
Textbooks:					
1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students” 2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”					
Reference Books:					
1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners” 2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007. 3. Mayall, “Industrial Design”, McGraw Hill, 1992. 4. Niebel, “Product Design”, McGraw Hill, 1974.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|--|
| <ol style="list-style-type: none">5. Asimov, “Introduction to Design”, Prentice Hall, 1962.6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”, 2016. |
|--|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS ANALOG IC DESIGN	L	T	P	C
21D57101		3	0	0	3
Semester		II			
Course Objectives:					
- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies. - Basic design concepts, issues and tradeoffs involved in analog IC design are explored. - Intuitive understanding and real-life applications are emphasized throughout the course. - To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp. - To know about Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.					
Course Outcomes (CO): Student will be able to					
- Design MOSFET based analog integrated circuits. - Analyze analog circuits at least to the first order. - Appreciate the trade-offs involved in analog integrated circuit design. - Understand and appreciate the importance of noise and distortion in analog circuits. - Analyze complex engineering problems critically in the domain of analog IC design for conducting research. - Solve engineering problems for feasible and optimal solutions in the core area					
UNIT - I	Lecture Hrs:				
Basic MOS Device Physics:General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.					
UNIT - II	Lecture Hrs:				
Differential Amplifiers: Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit					
UNIT - III	Lecture Hrs:				
Frequency Response of Amplifiers:General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.					
UNIT - IV	Lecture Hrs:				
Feedback Amplifiers:General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.					
UNIT - V	Lecture Hrs:				
Comparators:Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.					
Textbooks:					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
 (Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|--|
| 1. B.Razavi, “Design of Analog CMOS Integrated Circuits”, 2 nd Edition, McGraw Hill Edition 2016.
2. Paul.R.Gray & Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, 5 th Edition, 2009. |
|--|

Reference Books:

- | |
|---|
| 1. T.C. Carusone, D.A. Johns & K. Martin, “Analog Integrated Circuit Design”, 2 nd Edition, Wiley, 2012.
2. P.E. Allen & D.R. Holberg, “CMOS Analog Circuit Design”, 3 rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, “CMOS Circuit Design, Layout, and Simulation”, 3 rd Edition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, “Microelectronic Circuits”, 6 th Edition, Oxford University Press |
|---|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEMS DESIGN		L	T	P	C
21D06201			3	0	0	3
Semester			II			
Course Objectives:						
- To differentiate between a General purpose and an Embedded System. - To provide knowledge on the building blocks of Embedded System. - To understand the requirement of Embedded firmware and its role in API.						
Course Outcomes (CO): Student will be able to						
- Expected to differentiate the design requirements between General Purpose and Embedded Systems. - Expected to acquire the knowledge of firmware design principles. - Expected to understand the role of Real Time Operating System in Embedded Design. - To acquire the knowledge and experience of task level Communication in any Embedded System.						
UNIT - I					Lecture Hrs:	
Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.						
UNIT - II					Lecture Hrs:	
Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. DDR , Flash, NVRAM						
UNIT - III					Lecture Hrs:	
Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.						
UNIT - IV					Lecture Hrs:	
RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.						
UNIT - V					Lecture Hrs:	
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.						
Textbooks:						
1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.						
Reference Books:						
1. Embedded Systems - Raj Kamal, TMH.						
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.						
3. Embedded Systems – Lyla, Pearson, 2013						
4. An Embedded Software Primer - David E. Simon, Pearson Education.						



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PATTERN RECOGNITION AND MACHINE LEARNING	L	T	P	C
21D68201a		3	0	0	3
Semester		II			
Course Objectives:					
- To understand the mathematical formulation of patterns. - To study the various linear models. - To understand the basic classifiers. - To distinguish different models.					
Course Outcomes (CO):					
Student will be able to - Learn the basics of pattern classes and functionality. - Construct the various linear models. - Understand the importance kernel methods. - Learn the Markov and Mixed models.					
UNIT - I		Lecture Hrs:			
Introduction to Pattern recognition: Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization					
UNIT - II		Lecture Hrs:			
Linear Models: Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs , Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models - Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions					
UNIT - III		Lecture Hrs:			
Kernel Methods: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification					
UNIT - IV		Lecture Hrs:			
Graphical Models: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, Dseparation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.					
UNIT - V		Lecture Hrs:			
Mixture Models and EM algorithm: K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EMGaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
 (Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.
Textbooks:
1.Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press, volume no.52. 2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006.
Reference Books:
1.Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2 nd Ed., 2001. 2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

(Established by Govt. of A.P., ACT No.30 of 2008)

ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE	L	T	P	C
21D68201b		3	0	0	3
Semester		II			
Course Objectives:					
- To introduce students to various programming languages like C, C++,Java script, PERL, etc. - To distinguish between Procedural and OOP language, Introduce features of OOPs etc. - To demonstrate the development of some typical applications using different Programming languages.					
Course Outcomes (CO):					
Students will be able to:					
- Introduce students to various programming languages like C, C++,Java script, PERL, etc. - Distinguish between Procedural and OOP language, Introduce features of OOPs etc. - Demonstrate the development of some typical applications using different Programming languages.					
UNIT - I	Lecture Hrs:				
Embedded ‘C’ Programming: Bitwise operations, Dynamic memory allocation, OS services, linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimization issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods (Waterfall, Agile).					
UNIT - II	Lecture Hrs:				
Object Oriented Programming: Introduction to procedural, modular, object oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data Abstraction and information hiding, inheritance, polymorphism.					
UNIT - III	Lecture Hrs:				
CPP Programming: ‘cin’, ‘cout’, formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, ‘this’ pointer, constructors, destructors, friend function, dynamic memory allocation.					
UNIT - IV	Lecture Hrs:				
Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance. Templates: Function template and class template, member function templates and template arguments					
UNIT - V	Lecture Hrs:				
Exception Handling: Syntax for exception handling code: try-catch-throw, Multiple Exceptions. Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.					
Textbooks:					
1. Michael J. Pont , “Embedded C”, Pearson Education, 2ndEdition,2008 2.Robert Sedgewick, “Algorithms in C++”, Addison Wesley PublishingCompany, 1999.					
Reference Books:					
1. Randal L. Schwartz, “Learning Perl”, O’Reilly Publications, 6th Edition2011 2.Michael Berman, “Data structures via C++”, Oxford UniversityPress, 2002					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	RF IC DESIGN	L	T	P	C
21D68201c		3	0	0	3
Semester		II			
Course Objectives:					
- To introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc. - To demonstrate design of High Frequency Amplifiers. - To introduce various types of Power Amplifiers and PLLs					
Course Outcomes (CO):					
Students will be able to - Introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc. - Demonstrate design of High Frequency Amplifiers. - Introduce various types of Power Amplifiers and PLLs					
UNIT - I					Lecture Hrs:
RF Tuned Circuits: RF systems – Basic architectures, Maximum Power Transfer, Passive RLC Networks, Parallel RLC tank, Q, Series RLC networks, matching, Pi match, T match, Passive components in IC: Resistors, capacitors, Inductors, Transceiver Architectures.					
UNIT - II					Lecture Hrs:
Nonlinearity and Reflection Coefficient: Nonlinearity and Time Variance of system, sensitivity and dynamic range, Review of MOS Device Physics, MOS device review, Distributed Systems, Transmission lines, reflection coefficient, the wave equation Lossy transmission lines Smith charts – plotting gamma, Noise in FET: Thermal noise, flicker noise review					
UNIT - III					Lecture Hrs:
High Frequency Amplifier Design: Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise-time, delay and bandwidth, Zeros to enhance bandwidth, Shunt- series amplifiers, tuned amplifiers Cascaded amplifiers, Noise figure, Intrinsic MOS noise parameters, LNA Design, Power match versus noise match.					
UNIT - IV					Lecture Hrs:
RF Power Amplifiers: Multiplier based mixers, Subsampling mixers & Mixer Design, RF Power Large signal performance Amplifiers, Class A, AB, B, C amplifiers, Class D, E, F amplifiers, RF Power amplifier design issues.					
UNIT - V					Lecture Hrs:
PLL: Voltage controlled oscillators, Resonators, Negative resistance oscillators, Phase locked loops, Linearized PLL models, Phase detectors, charge pumps, Loop filters, PLL design examples, Frequency synthesis and oscillator Frequency division, integer-N synthesis, Fractional frequency synthesis, Phase noise.					
Textbooks:					
1. Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, Cambridge University Press, 2004.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

2.BehzadRazavi, “RF Microelectronics”, Prentice Hall, 1997.
Reference Books:
1. Abidi, P.R. Gray, and R.G. Meyer, eds., “Integrated Circuits for Wireless Communications”, New York: IEEE Press, 1999.
2.R. Ludwig and P. Bretchko, “RF Circuit Design, Theory andApplications”, Pearson, 2000



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SoC ARCHITECTURE	L	T	P	C
21D06203a		3	0	0	3
Semester		II			
Course Objectives:					
- To understand the basics related to SoC architecture and different approaches related to SoC Design. - To select an appropriate robust processor for SoC Design - To select an appropriate memory for SoC Design. - To realize real time case studies					
Course Outcomes (CO): Student will be able to					
- Understand the basics related to SoC architecture and different approaches related to SoC Design. - Select an appropriated robust processor for SoC Design - Select an appropriate memory for SoC Design. - Realize real time case studies					
UNIT - I	Lecture Hrs:				
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.					
UNIT - II	Lecture Hrs:				
Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors					
UNIT - III	Lecture Hrs:				
Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.					
UNIT - IV	Lecture Hrs:				
Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.					
SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.					
UNIT - V	Lecture Hrs:				
Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.					
Textbooks:					
1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.					
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.					
Reference Books:					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

(Established by Govt. of A.P., ACT No.30 of 2008)

ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|---|
| <ol style="list-style-type: none">1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer2.Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.3.System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers |
|---|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SYSTEM DESIGN WITH EMBEDDED LINUX	L	T	P	C
21D68202a		3	0	0	3
Semester		II			
Course Objectives:					
- To understand the importance of Embedded Linux in system design - To analyze the architecture of embedded Linux in detail - To explain the Linux BSP for a hardware platform - To develop and Debug the drivers in Embedded Linux					
Course Outcomes (CO):					
Students will be able to - Understand the importance of Embedded Linux in system design - Analyze the architecture of embedded Linux in detail - Explain the Linux BSP for a hardware platform - Develop and Debug the drivers in Embedded Linux					
UNIT - I					Lecture Hrs:
Introduction: Need of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions Embedded Linux Architecture, Kernel Architecture: Hardware Abstraction Layer (HAL), Memory Manager, Scheduler, File System, IO Subsystem, Networking Subsystems, IPC; User Space, Linux Start-Up Sequence.					
UNIT - II					Lecture Hrs:
Board Support Package: Inserting BSP in Kernel Build Procedure, the Boot Loader Interface, Memory Map, Interrupt Management, the PCI Subsystem, Timers, UART, and Power Management. Embedded Storage: Flash Map, Memory Technology Device, MTD Architecture, Embedded File Systems.					
UNIT - III					Lecture Hrs:
Embedded Drivers: Linux Serial Driver, Ethernet Driver, and I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules. Porting Applications: Architectural Comparison, Application Porting Roadmap.					
UNIT - IV					Lecture Hrs:
Real-Time Linux: Linux and Real-Time: Building and Debugging: Building the Kernel, Building the Root File System, Integrated Development Environment, Elementary Concepts of Debugging. Embedded Graphics: Graphics System, Introduction to Display Hardware.					
UNIT - V					Lecture Hrs:
uClinux: Linux on MMU - Less Systems, Program Load and Execution, Memory Management, File / Memory Mapping.					
Textbooks:					
1. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with Embedded Linux”, Wiley, 1st Edition, 2014. 2.Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.					
Reference Books:					
1. P Raghvan, Amol Lad, SriramNeelakandan, “EmbeddedLinux System Design and Development”, Auerbach Publications, 2005. 2.KarimYaghmour. “Building Linux Systems”, O’Reilly & Associates.2008.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PHYSICAL DESIGN AUTOMATION	L	T	P	C
21D57202		3	0	0	3
	Semester	II			
Course Objectives:					
• To understand relation between automation algorithms and constraints posed by VLSI technology. • To adopt algorithms to meet critical design parameters. • To design area efficient logics by employing different routing algorithms and shape functions. • To simulate and synthesis different combinational and sequential logics.					
Course Outcomes (CO): Student will be able to					
• Understand relation between automation algorithms and constraints posed by VLSI technology. • Adopt algorithms to meet critical design parameters. • Design area efficient logics by employing different routing algorithms and shape functions. • Simulate and synthesis different combinational and sequential logics.					
UNIT - I		Lecture Hrs:			
VLSI Design Automation Tools: Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.					
UNIT - II		Lecture Hrs:			
Layout: Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.					
UNIT - III		Lecture Hrs:			
Floor planning and routing: Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.					
UNIT - IV		Lecture Hrs:			
Simulation and Logic Synthesis: Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.					
UNIT - V		Lecture Hrs:			
High-Level Synthesis: Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.					
Textbooks:					
1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998. 2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.					
Reference Books:					
1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999. 2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	CMOS ANALOG IC DESIGN LAB	L	T	P	C
21D57105		0	0	4	2
Semester		II			
Course Objectives:					
- To explain the VLSI Design Methodologies using VLSI design tool. - To grasp the significance of various CMOS analog circuits in full-custom IC Design flow - To explain the Physical Verification in Layout Design - To fully appreciate the design and analyze of analog and mixed signal simulation - To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation					
Course Outcomes (CO):					
- Explain the VLSI Design Methodologies using VLSI design tool. - Grasp the significance of various CMOS analog circuits in full-custom IC Design flow - Explain the Physical Verification in Layout Design - Fully appreciate the design and analyze of analog and mixed signal simulation - Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation					
List of Experiments:					
- The students are required to design and implement any TEN Experiments using CMOS 130nm Technology. - The students are required to implement LAYOUTS of any SIX Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation. - MOS Device Characterization and parametric analysis - Common Source Amplifier - Common Source Amplifier with source degeneration - Cascode amplifier - Simple current mirror - Cascode current mirror. - Wilson current mirror. - Differential Amplifier - Operational Amplifier - Sample and Hold Circuit - Direct-conversion ADC - R-2R Ladder Type DAC					
Lab Requirements:					
Software:					
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator					
Hardware:					
Personal Computer with necessary peripherals, configuration and operating System.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEM DESIGN LAB	L	T	P	C
21D06205		0	0	4	2
Semester		II			
Course Objectives:					
- To familiarize with embedded systems programming concepts - To implement different embedded communication and interfacing protocols					
Course Outcomes (CO):					
- Familiarize with embedded systems programming concepts - Implement different embedded communication and interfacing protocols					
List of Experiments:					
1. Functional Testing of Devices Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages. 2. Exporting Display on to other Systems Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server. 3. GPIO Programming Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality. 4. Interfacing Chronos eZ430 Chronos device is a programmable Texas Instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices. 5. ON/OFF Control Based On Light Intensity Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value. 6. Battery Voltage Range Indicator Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 LEDs, turn on 3 LED s for 2-3V, 2 LEDs for 1-2V, 1 LED for 0.1-1V & turn off all for 0V) 7. Dice Game Simulation Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game. 8. Displaying RSS News Feed On Display Interface Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet. 9. Porting Open w.r.t the Device Attempt to use the device while connecting to a WiFi network using a USB dongle and at the same time providing a wireless access point to the dongle. 10. Hosting a website on Board Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website. 11. Webcam Server					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. FM Transmission

Transforming the device into a regular FM transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Software Requirements:

Keil / Python

Hardware Requirements:

Arduino/Raspbery Pi/Beaglebone


JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

(Established by Govt. of A.P., ACT No.30 of 2008)

ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD
COMMON COURSE STRUCTURE & SYLLABI

Course Code	ADHOC AND WIRELESS SENSOR NETWORKS	L	T	P	C
21D06204b		3	0	0	3
Semester		III			
Course Objectives:					
- To understand the various wireless networks - To analyze MAC, routing and transport layer protocols - To learn about the concepts of wireless sensor networks					
Course Outcomes (CO):					
Students will be able to					
- Understand the various wireless networks - Analyze MAC, routing and transport layer protocols - Learn about the concepts of wireless sensor networks					
UNIT - I	Lecture Hrs:				
Wireless LANs and PANs: Introduction, Fundamentals of WLANs, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.					
AD HOC WIRELESS NETWORKS: Introduction, Issues in Ad Hoc Wireless Networks					
UNIT - II	Lecture Hrs:				
MAC Protocols: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.					
UNIT - III	Lecture Hrs:				
Routing Protocols: Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.					
UNIT - IV	Lecture Hrs:				
Transport Layer Protocols: Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other TransportLayer Protocol for Ad Hoc Wireless Networks.					
UNIT - V	Lecture Hrs:				
Wireless Sensor Networks: Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.					
Textbooks:					
1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B. S. Manoj, 2004, PHI.					
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control – JagannathanSarangapani, CRC Press.					
Reference Books:					
1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C. K. Toh, 1st Ed. Pearson Education.					
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	VLSI SIGNAL PROCESSING	L	T	P	C
21D57204c		3	0	0	3
Semester		II			
Course Objectives:					
- To study the existing architectures suitable for VLSI. - To understand the concepts of folding and unfolding algorithms and applications. - To design new architectures suitable for VLSI. - To implement fast convolution algorithms.					
Course Outcomes (CO): Student will be able to					
- Study the existing architectures suitable for VLSI. - Understand the concepts of folding and unfolding algorithms and applications. - Design new architectures suitable for VLSI. - Implement fast convolution algorithms.					
UNIT - I		Lecture Hrs:			
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques					
UNIT - II		Lecture Hrs:			
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.					
UNIT - III		Lecture Hrs:			
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.					
UNIT - IV		Lecture Hrs:			
Fast Convolution: Introduction – Cook - Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection					
UNIT - V		Lecture Hrs:			
Low Power Design: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches					
Text books:					
1.Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, Wiley Inter Science, 1998. 2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall, 1985.					
Reference Books					
1.Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994. 2. Mediseti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	IOT AND ITS APPLICATIONS	L	T	P	C
21D57204b		3	0	0	3
Semester		II			
Course Objectives:					
• To apply the Knowledge in IOT Technologies and Data management. • To determine the values chains Perspective of M2M to IOT. • To implement the state of the Architecture of an IOT. • To compare IOT Applications in Industrial & real world. • To demonstrate knowledge and understand the security and ethical issues of an IOT.					
Course Outcomes (CO): Student will be able to					
• Apply the Knowledge in IOT Technologies and Data management. • Determine the values chains Perspective of M2M to IOT. • Implement the state of the Architecture of an IOT. • Compare IOT Applications in Industrial & real world. • Demonstrate knowledge and understand the security and ethical issues of an IOT.					
UNIT - I	Lecture Hrs:				
Fundamentals of IoT: Evolution of Internet of Things, Enabling Technologies, IoT Architectures, oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of an IoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects. IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.					
UNIT - II	Lecture Hrs:				
IoT Protocols: IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.					
UNIT - III	Lecture Hrs:				
Design and Development: Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.					
UNIT - IV	Lecture Hrs:				
Data Analytics and Supporting Services: Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.					
UNIT - V	Lecture Hrs:				
Case Studies/Industrial Applications: IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).					
Textbooks:					
1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017. 2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madiseti, Universities					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
 (Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Press,2015
Reference Books:
1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2). 2. “From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence”, Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014. 3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011.



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

AUDIT COURSE-I



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
21DAC101a		2	0	0	0
Semester		I			
Course Objectives: This course will enable students:					
- Understand the essentials of writing skills and their level of readability - Learn about what to write in each section - Ensure qualitative presentation with linguistic accuracy					
Course Outcomes (CO): Student will be able to					
- Understand the significance of writing skills and the level of readability - Analyze and write title, abstract, different sections in research paper - Develop the skills needed while writing a research paper					
UNIT - I	Lecture Hrs:10				
1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity					
UNIT - II	Lecture Hrs:10				
Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization					
UNIT - III	Lecture Hrs:10				
Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.					
UNIT - IV	Lecture Hrs:9				
Key skills needed for writing a Title, Abstract, and Introduction					
UNIT - V	Lecture Hrs:9				
Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions					
Suggested Reading					
1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I] 2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press 3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman’sbook 4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	DISASTER MANAGEMENT	L	T	P	C
21DAC101b		2	0	0	0
Semester		I			
Course Objectives: This course will enable students:					
- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response. - Critically evaluatedisasterriskreduction and humanitarian response policy and practice from Multiple perspectives. - Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations - Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches,planningand programming in different countries, particularly their home country or the countries they work in					
UNIT - I					
Introduction: Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude. Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics					
UNIT - II					
Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,DroughtsandFamines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.					
UNIT - III					
Disaster Preparedness and Management: Preparedness: Monitoring of Phenomena Triggering ADisasteror Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.					
UNIT - IV					
Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. TechniquesofRiskAssessment,GlobalCo-OperationinRiskAssessmentand Warning, People’s Participation in Risk Assessment. Strategies for Survival.					
UNIT - V					
Disaster Mitigation: Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigationand Non-Structural Mitigation, Programs of Disaster Mitigation in India.					
Suggested Reading					
- R.Nishith,SinghAK,“DisasterManagementinIndia:Perspectives,issuesandstrategies “New Royal book					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

- | |
|---|
| <p>Company..Sahni,PardeepEt.AL.(Eds.),”DisasterMitigationExperiencesAndReflections”,PrenticeHall OfIndia, New Delhi.</p> <p>3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies”,Deep&Deep Publication Pvt. Ltd., New Delhi</p> |
|---|



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	SANSKRITFOR TECHNICAL KNOWLEDGE	L	T	P	C
21DAC101c		2	0	0	0
Semester		I			
Course Objectives: This course will enable students:					
- To get a working knowledge in illustrious Sanskrit, the scientific language in the world - Learning of Sanskrit to improve brain functioning - LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancing the memory power - The engineering scholars equipped with Sanskrit will be able to explore the huge - Knowledge from ancientliterature					
Course Outcomes (CO): Student will be able to					
- Understanding basic Sanskrit language - Ancient Sanskrit literature about science &technology can be understood - Being a logical language will help to develop logic in students					
UNIT - I					
Alphabets in Sanskrit,					
UNIT - II					
Past/Present/Future Tense, Simple Sentences					
UNIT - III					
Order, Introduction of roots					
UNIT - IV					
Technical information about Sanskrit Literature					
UNIT - V					
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics					
Suggested Reading					
1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi					
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication					
3.“India’s Glorious ScientificTradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

AUDIT COURSE-II



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PEDAGOGY STUDIES	L	T	P	C
21DAC201a		2	0	0	0
Semester		II			
Course Objectives: This course will enable students:					
- Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. - Identify critical evidence gaps to guide the development.					
Course Outcomes (CO): Student will be able to					
Students will be able to understand:					
- What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries? - What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners? - How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?					
UNIT - I					
Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.					
UNIT - II					
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.					
UNIT - III					
Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.					
UNIT - IV					
Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barrier to learning: limited resources and large class sizes					
UNIT - V					
Research gaps and future directions: Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.					
Suggested Reading					
- Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261. - Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379. - Curriculum Studies, 36 (3): 361-379.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teachereducation research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacherpreparation count?International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
Chavan M (2003)ReadIndia: A mass scale, rapid, ‘learning to read’campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	STRESSMANAGEMENT BY YOGA	L	T	P	C
21DAC201b		2	0	0	0
Semester		II			
Course Objectives: This course will enable students:					
- To achieve overall health of body and mind - To overcome stres					
Course Outcomes (CO): Student will be able to					
- Develop healthy mind in a healthy body thus improving social health also - Improve efficiency					
UNIT - I					
Definitions of Eight parts of yog.(Ashtanga)					
UNIT - II					
Yam and Niyam.					
UNIT - III					
Do`sand Don`t`s in life. i) Ahinsa,satya,astheya,bramhacharyaand aparigrahaii) Shaucha,santosh,tapa,swadhyay,ishwarpranidhan					
UNIT - IV					
Asan and Pranayam					
UNIT - V					
i)Variousyogposesand theirbenefitsformind &body ii)Regularizationofbreathingtechniques and its effects-Types ofpranayam					
Suggested Reading					
1.‘Yogic Asanas forGroupTarining-Part-I’: Janardan SwamiYogabhyasiMandal, Nagpur 2.“Rajayogaor conquering the Internal Nature” by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS	L	T	P	C
21DAC201c		2	0	0	0
Semester		II			
Course Objectives: This course will enable students:					
- To learn to achieve the highest goal happily - To become a person with stable mind, pleasing personality and determination - To awaken wisdom in students					
Course Outcomes (CO): Student will be able to					
- Study of Shrimad-Bhagwad-Geeta will help the student in developing his personality and achieve the highest goal in life - The person who has studied Geeta will lead the nation and mankind to peace and prosperity - Study of Neetishatakam will help in developing versatile personality of students					
UNIT - I					
Neetisatakam- Holistic development of personality Verses-19,20,21,22(wisdom) Verses-29,31,32(pride & heroism) Verses-26,28,63,65(virtue)					
UNIT - II					
Neetisatakam- Holistic development of personality Verses-52,53,59(dont's) Verses-71,73,75,78(do's)					
UNIT - III					
Approach to day to day work and duties. Shrimad Bhagwad Geeta: Chapter 2- Verses 41,47,48, Chapter 3- Verses 13,21,27,35, Chapter 6- Verses 5,13,17,23,35, Chapter 18- Verses 45,46,48.					
UNIT - IV					
Statements of basic knowledge. Shrimad Bhagwad Geeta: Chapter 2- Verses 56,62,68 Chapter 12 - Verses 13,14,15,16,17,18 Personality of Role model. Shrimad Bhagwad Geeta:					
UNIT - V					
Chapter 2- Verses 17, Chapter 3- Verses 36,37,42, Chapter 4- Verses 18,38,39 Chapter 18- Verses 37,38,63					
Suggested Reading					
1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata 2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P. Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

OPEN ELECTIVE



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	INDUSTRIAL SAFETY	L	T	P	C
21DOE301b		3	0	0	3
Semester		III			
Course Objectives:					
- To know about Industrial safety programs and toxicology, Industrial laws , regulations and source models - To understand about fire and explosion, preventive methods, relief and its sizing methods - To analyse industrial hazards and its risk assessment.					
Course Outcomes (CO): Student will be able to					
- To list out important legislations related to health, Safety and Environment. - To list out requirements mentioned in factories act for the prevention of accidents. - To understand the health and welfare provisions given in factories act.					
UNIT - I	Lecture Hrs:				
Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.					
UNIT - II	Lecture Hrs:				
Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.					
UNIT - III	Lecture Hrs:				
Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants- types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.					
UNIT - IV	Lecture Hrs:				
Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.					
UNIT - V	Lecture Hrs:				
Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance					
Textbooks:					
1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services. 2. Maintenance Engineering, H. P. Garg, S. Chand and Company.					
Reference Books:					
1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication. 2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	BUSINESS ANALYTICS		L	T	P	C
21DOE301c			3	0	0	3
Semester			III			
Course Objectives:						
The main objective of this course is to give the student a comprehensive understanding of business analytics methods.						
Course Outcomes (CO): Student will be able to						
- Students will demonstrate knowledge of data analytics. - Students will demonstrate the ability of think critically in making decisions based on data and deep analytics. - Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making. - Students will demonstrate the ability to translate data into clear, actionable insights.						
UNIT - I						Lecture Hrs:
Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst. Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.						
UNIT - II						Lecture Hrs:
Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.						
UNIT - III						Lecture Hrs:
Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents.Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling						
UNIT - IV						Lecture Hrs:
Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools						
UNIT - V						Lecture Hrs:
Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.						
Textbooks:						
1. Business Analysis by James Cadle et al. 2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray						
Reference Books:						
1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press. 2. Business Analytics by James Evans, persons Education.						



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

Course Code	WASTE TO ENERGY	L	T	P	C
21DOE301e		3	0	0	3
Semester		III			
Course Objectives:					
- Introduce and explain energy from waste, classification and devices to convert waste to energy. - To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process. - To educate on biogas properties ,bio energy system, biomass resources and their classification and biomass energy programme in India.					
Course Outcomes (CO): Student will be able to					
- To know about overview of Energy to waste and classification of waste. - To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion process in detail. - To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.					
UNIT - I	Lecture Hrs:10				
Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors					
UNIT - II	Lecture Hrs:10				
Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.					
UNIT - III	Lecture Hrs:12				
Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation					
UNIT - IV	Lecture Hrs:12				
Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.					
UNIT - V	Lecture Hrs:10				
Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.					
Textbooks:					
- Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018 - Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017					
Reference Books:					
- Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991. - Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley					



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
(Established by Govt. of A.P., ACT No.30 of 2008)
ANANTHAPURAMU – 515 002 (A.P) INDIA

M.TECH. IN VLSI&ES/ES&VLSI/VLSI&ESD

COMMON COURSE STRUCTURE & SYLLABI

& Sons, 1996
Online Learning Resources:
https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/ https://www.youtube.com/watch?v=x2KmjbCvKtk